



AUTOMATIC TEST SYSTEMS EXECUTIVE DIRECTORATE  
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From: DoD ATS Test Program Set Integrated Product Team  
To: DoD ATS Executive Directorate

Subj: Automatic Test System Lessons Learned

Encl: (1) Navy CASS Family Lessons Learned  
(2) Army IFTE Family Lessons Learned  
(3) ARGCS Lessons Learned

1. The DoD ATS Test Program Set Integrated Product Team (TPS IPT) was tasked by action item 3/09-1 to collect, organize and publish on the DoD ATS web site TPS rehost data from CASS, IFTE and ARGCS. This action item was to help the Air Force team prepare for rehosting TPSs onto the VDATS.

2. Please direct questions to Kevin Dusch at (301) 757-6888 (e-mail [Kevin.dusch@navy.mil](mailto:Kevin.dusch@navy.mil)).

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## Navy CASS Family Lessons Learned

1. Problem: Do not assume that the hardware and software specifications for the legacy ATS are correct. The CASS specification was too often misunderstood. CASS instruments were designed with built in headroom to ensure that they could meet the specifications across the operating environment. This headroom is not documented and while RTCASS was designed to meet the CASS specifications, it often fell short of the true CASS performance envelope. Often TPS developers use instruments to their full capabilities which exceeded the published specifications. TPS developers did not do this intentionally, but since the UUT test passed and all faults were properly detected and isolated, the TPS developers considered the task complete.
  - a. Solution Step 1: Define the legacy ATS
    - i. Characterize each instrument from the legacy ATS using parametric tests. Design a functional qualification test “Super TPS” to capture this data.
    - ii. Measure and document the steady-state performance of each instrument.
      1. Example: CASS DTU current output spec is 50mA, but typical output can be 70mA on CASS Block I. Measure and document the CASS minimum and maximum output for each legacy station configuration
    - iii. Measure and document the dynamic performance of each instrument. What is the slew rate for each instrument?
      1. Example: How long does it take to load and burst a digital pattern?
      2. Example: Arbitrary Waveform Generator (AWFG) half cycle mode.
      3. Example: Waveform Digitizer phase angle
      4. Example: Waveform Digitizer triggering, both simple and complex.
    - iv. Measure and document the quiescent state of each interface on a pin-by-pin basis. When the ATS is initialized, what is the logic state and impedance on each analog and digital I/O pin?
      1. Example: Do power supply output pins have isolation relays or are they directly connected to the interface?
    - v. Document the concurrent capabilities of each instrument.
      1. Example: CASS AWFG concurrent channel output and synchronization
      2. Example: CASS Communication interfaces (MS1553, RS-232, RS-422)
    - vi. Measure and document path switching characteristics and path losses. Sequence and timing of ATE switch closures are also very important.
      1. Example: DC path losses due to line length.
      2. Example: AC losses due to capacitive loading (ex. 39pF/ft for RG316 coax)
      3. Example: ATS relay switch closure timing and sequential order.
  - b. Solution Step 2: Analyze the new instruments in the proposed ATS; characterize each instrument to be used in the proposed ATS using parametric tests. Use a Functional Qualification Test (FQT) to capture this data.
    - i. Use subsets of the FQT to compare performance of the new instrument to the legacy instrument. Do not wait until the system design is complete to gather this data. Gather data early and often on individual instruments in order to select the optimum instrument.

- ii. Work with vendors to update specifications, and if necessary, correct the instrument performance.
  - iii. Complete the ATS Design Verification Tests (DVT) prior to TPS re-host so that problems are identified before they become too expensive to fix.
- 2. Problem: Test Programs too often have dependencies on both inter-statement timing, the time between each statement in a test sequence, and on intra-statement timing, the time it takes to execute a single step. These times are based on the system processor and the communication link to the instruments. New instruments may have more latency since they may have to transfer more information to control instrument features than the legacy instrument.
  - a. Solution:
    - i. Work with instrument vendors to reduce access and setup times in new instruments.
    - ii. Use state caching to minimize the communication to the instrument.
    - iii. Enable more synchronization between instruments.
    - iv. Enable parallel loading to reduce run time.
- 3. Problem: Legacy ATS instruments do not have compatible replacements.
  - a. Solution: Develop the baseline specification. Use data mining tools early in the program to determine instrument capabilities and make the new instrument selection process easier and more cost effective, then feed these changes back into the specification. The specification needs to be continuously updated through the life cycle of the ATS.
  - b. Solution:
    - i. RTConvert.exe can build a Program Identification Database (PID) that defines the envelope of the instrument.
    - ii. The Teradyne L2 Analyzer tool was developed to capture digital requirements, both hardware and language usage, in order to highlight risk areas.
    - iii. Eliminate unused instrument capabilities at the system level on both new and legacy instruments and close the gate on using these capabilities in new TPS development. Add new capabilities via a formal System Problem Report process.
      - 1. Example: CASS Microwave Transition Analyzer (MTA)
      - 2. Example: CASS MAC kit
- 4. Problem: The need for ATE ancillaries is not properly considered during TPS development and deployment. ATE ancillary items that could reduce TPS hardware complexity may not be available for TPS development in the quantities necessary for Fleet utilization.
  - a. Solution: Prior to contracting for TPS development, investigate the need for and availability of ATE ancillaries. If a desired ancillary is not available, ensure the TPS developer is advised that the ancillary can not be used for the development efforts. Need a position in the organization to look across TPS development efforts to harmonize ancillary equipment and make ancillaries part of the test system where appropriate.
- 5. Problem: Availability and accuracy of Unit Under Test (UUT) source data. Complete source data for older UUTs may not be found. Data that is available may not be current. Source data for newer UUTs may not have been procured.
  - a. Solution: Make a thorough examination of available source data. Simply stating "this is all the data the government has" and asking the contractor to bid the risk will always place the risk on the government simply because the product we receive back from the

contractor will only be as good as the data we give them. The Government should endeavor to always provide (at all costs) the latest data. If data does not exist or can not be obtained then one of the following approaches should be taken:

- i. Identify what data is missing so the TPS developer can knowingly “bid the risk” if Firm Fixed Price.
  - ii. Use a cost-reimbursable contract so that the TPS developer will be fairly compensated for their efforts.
  - iii. Develop the TPS organically
  - iv. Do not develop a TPS. Instead use a PBL contract or contract with the OEM for support.
6. Problem: Availability and configuration of Government Furnished Equipment (GFE) UUTs. Two each of a UUT configuration may not be available for TPS development. At times even one can not be made available. The UUT configuration that is provided may not be that which is in use in the Fleet.
  - a. Solution: Prior to contracting for TPS development, the availability of the correct configuration UUTs must be known. If UUTs can not be provided, then support should be established via PBL or OEM.
  - b. Solution: Start with the APML and Supply (ICP) community before going to the Maintenance - AIMDs, Depots, MOs, CNAF
  - c. Have a single POC for all GFE matters
7. Problem: Interface Devices (IDs) have been “overpopulated” in the past. In a competitive scenario, the cost effective approach for a TPS developer is have a large number of SRAs or WRAs on one ID. The design cost is reduced and, more importantly, production costs are reduced. For the Fleet user, overpopulation results in poor maintainability and poor production through-put.
  - a. Solution: Identify the heavy hitter UUTs - those UUTs that will be tested often. Populate the IDs based on Fleet utilization scenario. Even the non- heavy hitter UUTs should have no more than 3 WRAs and 10 SRAs on an ID in order to minimize ID population.
8. Problem: Government hasn't fully utilized the expertise of the fleet and/or the Fleet Support Team in the TPS development process.
  - a. Solution: Continue to work with the Fleet to get firm commitments for providing support throughout the TPS development process, especially focusing in on the problem areas of the UUT. Get the right person for each of the UUTs.
9. Problem: Engineering and logistics competency representatives do not stay on top of the development/review process as closely as required.
  - a. Solution: Make sure the engineering and logistics personnel maintain a close relationship with the contractor and review the data deliverables on time and provide timely responses, thus avoiding disagreements and costly reworks.
10. Problem: Program Managers did not accurately identify the UUTs that really needed to be Offloaded from legacy ATE based on actual failure rates/fleet inputs.
  - a. Solution: Thoroughly analyze historical data
11. Problem: Specification does not differentiate between new development versus offload TPSs or new avionics versus legacy avionics. Provide flexibility in the specification.
  - a. Solution: Add a statement that requirements may be deviated from when necessary and approved.

- i. Example: A specification is a one size fits all requirement for the entire program. The TPS developer should be able to easily meet all requirements for items they are developing. UUTs which may not have the all signals available for measurement impeding fault isolation. Many of our legacy TPSs could not comply with the current specifications without major rework.

12. Problem – Repair of GFE UUTs

- a. Solution: The government should coordinate all GFE UUT repairs. Sometimes all that is needed is an easily replaceable component which we can provide to the contractor. In most cases, the UUT will need to be shipped to a repair point since the contractor will most likely not have capability to repair or RFI the items.
- b. Establish a FEDEX shipping account to for UUTS - to and from repair.
- c. Make sure all GFE requirement dates are tied to milestone events, not calendar dates, in case schedule slips. This will avoid contract modifications.
- d. If only one UUT is provided, ensure that a replacement UUT can be obtained when one goes down to avoid stop work and claims. Some repairs can take six months.
- e. Make "Deviations" an applicable contract attachment so it won't be argued later by the Procuring Contracting Officer (PCO). Establish in writing how and who signs/approves the deviation.
- f. For schedule impacts, use "No fault - No foul". If it is not the contractors fault, do not ask for consideration. If it is their fault, require consideration.
- g. Establish a requirement for the developer to provide weekly a "tests integrated" e.g., total tests, overarching schedule, how many tests per week needed to hold schedule, and many tests actually performed. An Excel plot works fine.

13. Problem: Have an organizational structure that can handle geographically dispersed teams

- a. Solution: have summary meetings to brief the larger team and forge relationships
  - i. Technical Working Group – engineering focus to status all projects and upgrades happening to the ATE and TPSs. This is also a forum to have break-out sessions to address emerging problems
  - ii. Fleet Supportability Review – This enables the acquisition teams to meet and hear from the Fleet user. Provides great dialog on ATS use and potential improvements. Forges relationships with customer.

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## Army IFTE Family Lessons Learned

- 1 Problem: The newer (V)5 ATE may operate existing, reasonably non-complex, TPSs transitioned from the (V)3 without significant need for modification. However, once this transition is impacted by uses of the ATE assets in a more complex scenario, there are several areas which will be of immediate concern to the TPS designer. Review of the C/ATLAS Programmer's Manual will reveal distinct characteristics between the (V)3 Digital Word Generator (DWG) and the newer (V)5 Digital Test Interface (DTI, also referred to as the "DWG" in the Manual), but it is not completely comprehensive. By contrast, the Manual's Bus Test Unit (BTU) section does not indicate any distinction between the (V)3 version and the newer (V)5 version, but other documents exist which detail the significant design differences which must be accounted for in any conversion effort. Beyond these there exist more subtle items which require design attention to accomplish any conversion effort. In addition to potential software changes, (for example those required to make the (V)5 BTU accomplish the same tasks as the prior (V)3 BTU), there may be a requirement for (V)3-compatible Minor Adapter (ICD) hardware changes to permit a TPS to work on the (V)5. It is a foregone conclusion of this document that the designer will prefer to keep any such hardware changes to a bare minimum and will plan for requisite costs associated with these changes to include sufficient investigation and integration time.
  - a Solution Step 1: Determining Potential Incompatibilities - the potential incompatibilities between the (V)3 and (V)5 ATEs must be assessed for possible software and hardware implications.
    - i Normal test execution may be accomplished as far as possible to determine issues arising from inherent ATE differences. It has been a common experience with the (V)5 that many tests transitioned from the (V)3 which simply measure such characteristics as resistance, voltage, or signal timing and do not involve critical timing, loading, or multiple-state circumstances may perform quite readily on the V(5).
    - ii It will be necessary to determine the requirement for any of the interface elements below and document any ATE error outputs (this may be accomplished using the debug capabilities of the Run-Time system) during any preliminary execution of (V)3-compatible TPSs on the (V)5 ATE.
      - 1 The 1553 (BTU) Interface has specific new requirements for implementation on the (V)5 ATE. The use of the (V)5 BTU using (V)3 code constraints, (and perhaps an ICD hardware implementation circumstance), may result in the loss of 1553 communications with the UUT.
      - 2 If there is a requirement for an Ethernet interface, physical connection of the cables may interfere with normal operation of the TPS.
      - 3 If the use of the DWG asset is known to be relatively simple (meaning that there are not instances of use requiring critical timing, loading, or other more complex characteristics), tests may execute on the (V)5 quite similarly to their execution on the (V)3. If failures are encountered, however, this issue of complexity may be at the center of the issue.
      - 4 Due in part to the differences between grounding schemes in the (V)3 and (V)5 ATEs, and to the connectivity changes from the Virtual Instrument (VI) approach of the (V)3 and the VMEbus extensions for instrumentation (VXI) connections of the

- (V)5, any issues encountered which are not explainable in light of the above items will require more detailed investigation.
- 5 During integration of one of the Kiowa TPSs on the (V)5 a new revision to the BTU VXI instrument was delivered for the ATE. This new revision was found to have electrical characteristics which required additional accommodations in the converted TPS.
- b Solution Step 2: Determination of Actual Incompatible Test Strategies
- i Establish a baseline of tests which may be performed on either the (V)5 or the (V)3 using the existing ICD and TPS code. This may require additional effort to move around in the code and not execute previously failing tests, so this step may be quite extensive.
  - ii Review failures encountered during preliminary test operation and determine areas which may require special attention, in particular the following:
    - 1 If the TPS requires the use of the BTU for 1553 communication, the designer must modify the code to accommodate the requirements of the (V)5 BTU device.
      - (a) The difference between the (V)5 and (V)3 in the normal 1553 context is minimal, having to do with requiring the specification of a "16-BIT WORD LENGTH" in the SETUP, EXCHANGE statement for the (V)5 instrument. This additional specification will not interfere with functionality of the (V)3 SETUP.
      - (b) The differences are considerably greater if the designer must deal with 1553-bus error injection. In this latter case it will be necessary to consult a specific table of required and allowable error communication with which the (V)5 BTU can deal. This code change will be in addition to the required (V)3 methodology in cases where operation of an ICD on both a (V)3 and (V)5 ATE is necessary.
      - (c) It was discovered during one particular integration activity that the design of the 1553 bus in the ICD may become an issue on its own. While the (V)3 will accommodate a transformer-coupled bus in the ICD quite readily, it is now apparent that the (V)5 BTU only exists in a direct-coupled mode. If taken into account early enough in the TPS design process, it is possible that a selectable bus structure, (i.e., where if on a (V)3, the transformer coupling is implemented, while if on a (V)5, the direct coupling schema will be used), might be adopted. However, if a standard 1553B transformer coupling strategy has been employed for the (V)3 in the ICD, it should operate on the (V)5 as long as the maximum peak-to-peak signal level is not excessive. (The available (V)5 BTU specification limits any voltage value placed in the SETUP, EXCHANGE structure to +/-4.1V prior to any actual I/O activity by the BTU.)
    - 2 The (V)3 ATE requires use of a BNC 10-Base 2 connection preferably to the J5 connection on the back of the Peripheral Interface Controller (PIC). The (V)5 ATE has a 10-Base T modular connection present on the face of the I/O panel above the Analog and SDS interface instrument bays. It is possible to continue use of the 10-Base 2 connection if the BNC connector on the router in the rear of the utility cabinet of the (V)5 is not already in use.
    - 3 The majority of time in assessing the impacts of asset utilization between the (V)3 and (V)5 ATEs in all likelihood will be spent with the Digital Word Generator/

Digital Test Instrument. There are a variety of issues which have potential impacts on a compatibility effort.

- (a) The DWG in the (V)5 has been found to exhibit an increase in execution time per DO, DIGITAL event of approximately 20 times that of the (V)3. This is extremely significant if any extensive repetitive digital communication is accomplished in a loop structure. It is entirely possible that a particular TPS function will not complete in a timely manner (or at all if extensive enough), unless the code can be changed to accommodate a more continuous structure. In simple terms, for example, the first of the following use the DWG to send 10 STIM patterns repetitively one event at a time (four STIM pins sending, four RESP pins receiving). The second structure sends all 40 STIMs, and receives all 40 RESPs as one continuous event. (Note: For the first example 'I' is an INT type, 'FOUR\_STIMS' and 'FOUR\_RESPONSES' are DIGITAL types of 4 bits each and the "PINn" constants are INTERFACE declarations. 'TEMP\_STORE' is a DIGITAL array of 40 elements, 4 bits per element. In the second example 'FOUR\_STIMS' and 'FOUR\_RESPONSES' are arrays of type DIGITAL with 10 elements of 4 bits each)

(i) Example 1:

```
FOR, 'I' = 1 THRU 10, THEN $
DO, DIGITAL TEST USING 'DWG', STIM-RESP-SAVE,
  STIM 'FOUR_STIMS', RESP 'FOUR_RESPONSES'
  CNX-STIM PIN1 PIN2 PIN3 PIN4, CNX-STIM PIN5 PIN6 PIN7 PIN8
  $
CALCULATE, 'TEMP_STORE'('I') = 'FOUR_RESPONSES' $
END, FOR $
```

(ii) Example 2:

```
DO, DIGITAL TEST USING 'DWG', STIM-RESP-SAVE,
  STIM 'FOUR_STIMS'(1 THRU 10), RESP 'FOUR_RESPONSES' (1
  THRU 10)
  CNX-STIM PIN1 PIN2 PIN3 PIN4, CNX-STIM PIN5 PIN6 PIN7 PIN8
  $
END, FOR $
```

- (b) Discussion: It will take Example 1 approximately 10 seconds to execute, (depending upon the STIM-INTERVAL this might be even longer), while Example 2 will take closer to 10 times the STIM-INTERVAL set for this action). Clearly whenever such a change of approach is possible, execution time for DWG events may be improved. In many cases which are timing-dependent, such savings may overcome TPS failures on the (V)5.
- (c) DWG Frequency Generation: The (V)3 will output a continuous frequency given a code structure such as found below, (this has the effect of producing a "frequency shift" pattern which is continuous from lower to higher):

Enclosure (2)

Use of DWG to produce a continuous frequency output for input to a Phase Locked Loop device:

```
C
*****      MUST STEP UP FREQUENCY SLOWLY FOR PROPER OPERATION
*****
$
70.5 Hz      SETUP, DIGITAL TEST USING 'DWG', STIM-INTERVAL 1.0911E-3 SEC $
              DO, DIGITAL TEST USING 'DWG', STIM-ONLY, STIM 'HI_FREQ'(1 THRU
13),
              CIRCULATE CONTINUOUSLY, CNX-STIM J2-97 $
              DELAY, 0.2 SEC $
71.5 Hz      SETUP, DIGITAL TEST USING 'DWG', STIM-INTERVAL 1.0758E-3 SEC $
              DO, DIGITAL TEST USING 'DWG', STIM-ONLY, STIM 'HI_FREQ'(1 THRU
13),
              CIRCULATE CONTINUOUSLY, CNX-STIM J2-97 $
              DELAY, 0.2 SEC $
72.5 Hz      SETUP, DIGITAL TEST USING 'DWG', STIM-INTERVAL 1.0610E-3 SEC $
              DO, DIGITAL TEST USING 'DWG', STIM-ONLY, STIM 'HI_FREQ'(1 THRU
13),
              CIRCULATE CONTINUOUSLY, CNX-STIM J2-97 $
              DELAY, 0.2 SEC $
73.5 Hz      SETUP, DIGITAL TEST USING 'DWG', STIM-INTERVAL 1.0466E-3 SEC $
              DO, DIGITAL TEST USING 'DWG', STIM-ONLY, STIM 'HI_FREQ'(1 THRU
13),
              CIRCULATE CONTINUOUSLY, CNX-STIM J2-97 $
              DELAY, 0.2 SEC $
74.5 Hz      SETUP, DIGITAL TEST USING 'DWG', STIM-INTERVAL 1.0325E-3 SEC $
              DO, DIGITAL TEST USING 'DWG', STIM-ONLY, STIM 'HI_FREQ'(1 THRU
13),
              CIRCULATE CONTINUOUSLY, CNX-STIM J2-97 $
              DELAY, 0.2 SEC $
75.5 Hz      SETUP, DIGITAL TEST USING 'DWG', STIM-INTERVAL 1.0188E-3 SEC $
              DO, DIGITAL TEST USING 'DWG', STIM-ONLY, STIM 'HI_FREQ'(1 THRU
13),
              CIRCULATE CONTINUOUSLY, CNX-STIM J2-97 $
              DELAY, 0.2 SEC $
76.5 Hz      SETUP, DIGITAL TEST USING 'DWG', STIM-INTERVAL 1.0055E-3 SEC $
              DO, DIGITAL TEST USING 'DWG', STIM-ONLY, STIM 'HI_FREQ'(1 THRU
13),
              CIRCULATE CONTINUOUSLY, CNX-STIM J2-97 $
              DELAY, 0.2 SEC $
77.5 Hz      SETUP, DIGITAL TEST USING 'DWG', STIM-INTERVAL 9.9256E-4 SEC $
              DO, DIGITAL TEST USING 'DWG', STIM-ONLY, STIM 'HI_FREQ'(1 THRU
13),
              CIRCULATE CONTINUOUSLY, CNX-STIM J2-97 $
```

- (d) Discussion: On the (V)5, however, the DWG will “reset” with each “SETUP”, and therefore some alternative device must be utilized to duplicate this approach. In one specific instance this was accomplished by use of a Programmable Logic Device to output a varying frequency based on a simple 3-bit input code plus one code to allow automatic output of a fixed set of frequencies.
- (e) Occurrences of handshake use in the TPS potentially present a failure source. There is a difference in the timing with respect to the HANDSHAKE RESUME function between the (V)3 and the (V)5. On the former, the RESUME exhibits a reasonably steady relationship to the presence of valid data at the DWG input. On the (V)5, however, this relationship may be characterized as unpredictable to some degree. Therefore a new approach, including perhaps a timing delay device, will need to be considered if issues occur when using the DWG HANDSHAKE function on the (V)5 ATE. In addition to the above, the designer must be aware that the DWG on the (V)5 does not handle TIMING GROUP relationships in the same manner as the (V)3, (as the DTI is not divided into the same 16-DWG pin-groups as is true for the (V)3). When on the (V)5, the designer must be aware that multiple timing group programming is not possible. Likewise, once a specific group characteristic (whether timing or voltage) is programmed, all groups numerically above that being programmed will exhibit the same characteristic.
- (f) The designer must be aware that the (V)3 DWG exhibits a 95-ohm load to attached circuits, while the (V)5 will present a 50-ohm load. This may have consequences depending upon the type of device being interfaced.
- (g) The B-STIM CLOCK signal from the (V)3 DWG is a square wave with the falling edge being coincident with the DO, DIGITAL statement execution (on the next following master clock falling edge). On the (V)5 the B-STIM CLOCK signal is a short (< .1 micro-second), negative-going pulse. This may have an impact on the design of a critical-timing circuit associated with the DWG. It was found, however, that this has the advantage of being immediately usable for devices requiring a negative-going slope to trigger some form of digital signal (as with a UART).
- (h) It is of great significance in many LRU-related test environments to understand that, unlike the (V)3 DWGs, the (V)5 version of the digital interface may “wake up” in a totally unpredictable state. The designer must take the time to assess the need for a particular LRU input/output connection to be controlled at the initial state. It is highly recommended that the following structure be used at the initial point of each major segment of the TPS.
  - (i) Example:

```
CONNECT, DIGITAL TEST USING '<requirement>', CNX-BUS D1:192 $
DISCONNECT, DIGITAL TEST USING '<requirement>' CNX-BUS D1:192 $
```

- (ii) Discussion: In connection with the above concern, it must be noted that the REMOVE, ALL \$ ATLAS structure does not have the effect of removing connectivity to the DWGs nor does it return them to a quiescent state

c Solution Step 3: Updating the TPS to Incorporate Required Modifications

- i This step is predicated upon an understanding of the failures encountered and the apparent causal relationships. In broad terms, any issues discovered require specific knowledge of the electrical characteristics being tested in order to overcome the ATE differences.
  - ii Code changes have been found to be quite extensive during the compatibility efforts already conducted. Those items requiring established, documented updates were accomplished first and then tested extensively. More subtle code changes, such as awareness of the need for DELAY statements in the (V)5 code to allow for the greater execution time, may take longer to investigate and derive appropriate actions.
  - iii Hardware changes in the ICD will require the greatest design time, drawing changes, and associated build/debug effort.
- 2 Problem: The forward compatibility of some TPS hardware designs depends in part on the assumption that newer ATE designs will execute test statements at least as fast if not faster than the legacy ATE. However a “DO, DIGITAL...” statement executed on the V(5) was found to be 35 times slower than on the V(3) (1050msec vs. 30msec required to execute the statement). The serial communications tests in the Kiowa Warrior Internal Multiplexer Electronics Assembly (IEA) TPS as designed required one “DO, DIGITAL...” statement per digital word transmitted or received. This resulted in impractical run times for the TPS when ran on the V(5) due to the large number of digital words transferred (4096 words X 1050msec = 1.2 hours on V5 vs. 4096 words X 30msec = 2.05 minutes on V(3)). There were several such transfers in this TPS which already took about 1.5 hours to run on the V(3).
  - a Solution: The serial communication circuitry in the IEA TPS hardware was changed to a handshake configuration so that the number of “DO, DIGITAL...” statements could be greatly reduced. This resulted in a total test run-time of approx. 30 minutes on the V(3) compared with 1.5 hours before. Note: Changes in the V(5) Operating System have since improved the “DO, DIGITAL...” statement execution speed but it is still approximately 10 times slower than on the V3.
    - i Recommendation: Benchmark tests should be performed on each test instrument in both the legacy and new ATE prior to the start of future TPS rehost efforts. This will help in developing more accurate rehost cost estimates to provide to the customer. A test to compare the “DO, DIGITAL...” statement execution speed would have been helpful because the ATE specification does not provide any visibility into the time required for the execution of each test statement.
- 3 Problem: Many LRUs require multiple power inputs at various voltages. In normal operation these inputs are supplied simultaneously due to the fact that the various voltages are derived from a single source. In a typical testing scenario, the ATE supplies the power from independent power supplies which are applied in a serial fashion by the test program. A delay of approximately 0.1 second has been measured between the output of successive DC power supplies in the IFTE V(3). This delay has been shown to be due more to latency in the instrument or in communication with the instrument rather than the speed of the ATE processor. The delay causes one side of bipolar power inputs to be powered up for a short time (~0.1sec) while the other side is not. It is not known whether this puts stress on the circuitry but observed results have shown that this can cause Power-On Reset pulses and Power-On discrete signals to be out of spec.
  - a Solution: Although not a perfect solution, the impact of this issue has been minimized by experimenting with the order of power application (eg. -15VDC, +15VDC, +5VDC instead

- of +5VDC, +15VDC, -15VDC). A complete but more costly solution would be to incorporate relays in the TPS to apply power only when all power supplies were up.
- i Recommendation: Some older legacy ATE incorporated a Master Apply function (or similar function) to simultaneously apply previously setup stimuli. The “DO, SIMULTANEOUS” statement in the IEEE Standard C/ATLAS Test Language would provide this function but it is not incorporated into the ATLAS that resides on the IFTE. This would probably require modification to the ATE hardware.
- 4 Problem: Instrument behavior is seldom specified. Instrument behaviors often allow a TPS to work. This is often unknown and not intentional but sometimes the TPS engineer will discover a behavior and take advantage of it. For some behaviors it could be argued whether some utilizing it is right or wrong, but some behaviors are simply the way the instrument inherently works such as an unspecified rise time or execution time.
- a Example: Behaviors that are not captured in the IFTE instrument specifications.
    - i The IFTE V(3) AFG output is continuous but the V(5) AFG output is discontinuous when changing waveforms. On the V(5) this causes a gap in AFG output if you setup a waveform and then later setup the AFG to change the waveform. This happens because the V(5) AFG is designed to open the instrument's output relay at the beginning of every SETUP statement and close it when the SETUP programming is complete. The output will be zero when the relay is open. This is a safety feature not present in the previous V(3) AFG design. On the V(3) you could change a waveform parameter without losing the output signal.
    - ii DMM behavior is how the IFTE V(3) and V(5) DMM handled pulsed DC. The V(3) would return the Average DC Measurement for a Pulsed DC Signal. We have a TPS that takes advantage of that. The V(5) DMM lacks a capacitor to hold the peaks of pulsed DC and therefore the measurement is highly dependent on the sampling rate which was different among the different revisions of the DMM card.
  - b Solution: The instrument behavior should be characterized and documented when possible.

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## **ARGCS Joint Service Lessons Learned**

- 1 Problem with providing the most up-to-date source code to the contractor along with all the files. Had to make three different deliveries of the APG-60 Receiver/Exciter code.
- 2 Overall the contractor did a very good job with the Navy TPSs. They did track problems using test groups and provided a weekly summary of their efforts.
  - a The contractor had their own analysis tool, which they used.
  - b TPS ran a lot slower in the beginning of integration testing, but once changes to the drivers were accomplished they matched CASS TPS test times.
  - c Performed limited fault insertions to the WRAs with all faults inserted being detected.
  - d Uncovered that some of the original TPSs had code or tests that were not programmed correctly.
  - e The DMM was an issue and we had to make some changes based on the particular DMM being used.
  - f Because we were a demonstration program, we provided the contractor with more leeway to make TPS changes than we would have in a production program like RTCASS.
- 3 The Marine Corps did not insert faults in their tests. We used LRUs with real faults from the field.
  - a ATS-2 found the faults in the LRUs. We did not have time to test all the 60 plus LRUs we had.
- 4 Expect to find problems; the contractor uncovered a test in one of our programs that was not being tested correctly. They fixed that test and wrote a paper on the problem.

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