

DEFENSE ADVANCED RESEARCH PROJECTS AGENCY
FY2004 STTR Proposal Submission

DARPA's charter is to help maintain U.S. technological superiority over, and to prevent technological surprise by, its potential adversaries. Thus, the DARPA goal is to pursue as many highly imaginative and innovative research ideas and concepts with potential military and dual-use applicability as the budget and other factors will allow.

DARPA has identified technical topics to which small businesses may respond in the fiscal year (FY) 2004 STTR solicitation. Please note that these topics are UNCLASSIFIED and only UNCLASSIFIED proposals will be entertained. Although they are unclassified, the subject matter may be considered to be a "critical technology." If you plan to employ NON-U.S. Citizens in the performance of a DARPA STTR contract, please inform the Contracting Officer who is negotiating your contract. These are the only topics for which proposals will be accepted at this time. A list of the topics currently eligible for proposal submission is included followed by full topic descriptions. The topics originated from DARPA technical program managers and are directly linked to their core research and development programs.

NEW REQUIREMENT: ALL PROPOSAL SUBMISSIONS TO DARPA MUST BE SUBMITTED ELECTRONICALLY. PROPOSALS WHICH ARE NOT SUBMITTED THROUGH THE ON-LINE WEBSITE WILL NOT BE ACCEPTED.

It is mandatory that the complete proposal submission -- DoD Proposal Cover Sheet, **ENTIRE** Technical Proposal with any appendices, Cost Proposal, and the Company Commercialization Report -- be submitted electronically through the DoD SBIR website at <http://www.dodsbir.net/submission>. Each of these documents is to be submitted separately through the website. Your complete proposal **must** be submitted via the submissions site on or before the **6:00am EST, 15 April 2004 deadline**. **A hardcopy is no longer required.** A checklist has been prepared to assist small business activities in responding to DARPA topics. If you have any questions or problems with electronic submission, contact the DoD SBIR Help Desk at 1-866-724-7457 (8am to 5pm EST).

Acceptable Format for On-Line Submission: All technical proposal files must be in Portable Document Format (PDF) for evaluation purposes. The Technical Proposal should include all graphics and attachments but should not include the Cover Sheet or Company Commercialization Report (as these items are completed separately). Cost Proposal information should be provided by completing the on-line Cost Proposal form. This itemized listing should be placed as the last page(s) of the Technical Proposal Upload. (Note: Only one file can be uploaded to the DoD Submission Site. Ensure that this single file includes your complete Technical Proposal and the additional cost proposal information.)

Technical Proposals should conform to the limitations on margins and number of pages specified in the front section of this DoD solicitation. However, your cost proposal will only count as one page and your Cover Sheet will only count as two, no matter how they print out after being converted. Most proposals will be printed out on black and white printers so make sure all graphics are distinguishable in black and white. It is strongly encouraged that you perform a virus check on each submission to avoid complications or delays in submitting your Technical Proposal. To verify that your proposal has been received, click on the "Check Upload" icon to view your proposal. Typically, your proposal will be uploaded within the hour. However, if your proposal does not appear after an hour, please contact the DoD Help Desk.

DARPA recommends that you complete your submission early, as computer traffic gets heavy near the solicitation closing and slows down the system. **Do not wait until the last minute.** DARPA will not be responsible for proposals being denied due to servers being "down" or inaccessible. Please assure that your e-mail address listed in your proposal is current and accurate. By the end of April, you will receive an e-mail acknowledging receipt of your proposal.

PLEASE DO NOT ENCRYPT OR PASSWORD PROTECT TECHNICAL PROPOSAL

HELPFUL HINTS:

1. Consider the file size of the technical proposal to allow sufficient time for uploading.
2. Perform a virus check.

3. Signature is no longer required at the time of submission.
4. Submit a new/updated Company Commercialization Report.
5. Please call the Toll Free SBIR Help Desk if you have submission problems: 866-724-7457
6. DARPA will not accept proposal submissions by electronic facsimile (fax) or email.

Additional DARPA requirements:

- DARPA Phase I awards will be Firm Fixed Price contracts.
- Phase I proposals **shall not exceed \$99,000**, and may range from 8 to 12 months in duration. Phase I contracts cannot be extended.
- DARPA Phase II proposals must be invited by the respective Phase I DARPA Program Manager (with the exception of Fast Track Phase II proposals – see Section 4.5 of this solicitation). Phase 2 invitations will be based on the technical results reflected in the Phase I draft and/or final report as evaluated by the DARPA Program Manager utilizing the criteria in Section 4.3. DARPA Phase II proposals must be structured as follows: the first 10-12 months (base effort) should be approximately \$375,000; the second 10-12 months of incremental funding should also be approximately \$375,000. The entire Phase II effort should generally not exceed \$750,000.

Prior to receiving a contract award, the small business **MUST** be registered in the Centralized Contractor Registration (CCR) Program. You may obtain registration information by calling 1-888-227-2423 or Internet: <http://www.ccr.gov>.

The responsibility for implementing DARPA's Small Business Technology Transfer (STTR) Program rests with the Contract Management Office. The DARPA SBIR/STTR Program Manager is Connie Jacobs, see address below. DARPA invites small businesses, in cooperation with a researcher from a university, an eligible contractor-operated federally funded research and development center (FFRDC), or a non-profit research institution, to submit proposals thru the DoD website www.dodsbir.net/submission.

DEFENSE ADVANCED RESEARCH PROJECTS AGENCY

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STTR proposals submitted to DARPA will be processed by DARPA and distributed to the appropriate technical office for evaluation and action.

DARPA selects proposals for funding based on technical merit and the evaluation criteria contained in this solicitation document. DARPA gives evaluation criterion a., "The soundness, technical merit, and innovation of the proposed approach and its incremental progress toward topic or subtopic solution" (refer to section 4.2 Evaluation Criteria - Phase I - page 7), twice the weight of the other two evaluation criteria. **TRANSITION OF THE PROPOSED EFFORT IS VERY, VERY IMPORTANT. THE SMALL BUSINESS SHOULD INCLUDE THEIR TRANSITION VISION IN THEIR COMMERCIALIZATION STRATEGY. THE SMALL BUSINESS MUST UNDERSTAND THE END USE OF THEIR EFFORT AND THE END USER, i.e., ARMY, NAVY, AF, SOCOM, ETC.**

As funding is limited, DARPA reserves the right to select and fund only those proposals considered to be superior in overall technical quality and highly relevant to the DARPA mission. As a result, DARPA may fund more than one proposal in a specific topic area if the technical quality of the proposal(s) is deemed superior, or it may not fund any proposals in a topic area. Each proposal submitted to DARPA must have a topic number and must be responsive to only one topic.

- Cost proposals will be considered to be binding for 180 days from closing date of solicitation.
- **Successful offerors will be expected to begin work no later than 30 days after contract award.**
- For planning purposes, the contract award process is normally completed with 45 to 60 days from issuance of the selection notification letter to Phase I offerors.

**DARPA FY2004 Phase I STTR
Checklist**

Page Numbering

Number all pages of your proposal consecutively _____

Total for each proposal is 25 pages inclusive of cost proposal and resumes.

Beyond the 25 page limit do not forward appendices, attachments and/or additional references.

Company Commercialization Report **IS NOT** included in the page count

Proposal Format

b. Cover Sheet, Technical and Cost proposals, and Company Commercialization Report **MUST** be submitted electronically _____

c. Identification and Significance of Problem or Opportunity _____

d. Phase I Technical Objectives _____

e. Phase I Work Plan _____

f. Related Work _____

g. Relationship with Future Research and/or Development _____

h. Commercialization Strategy _____

i. Key Personnel, Resumes _____

j. Facilities/Equipment _____

k. Consultants _____

l. Prior, Current, or Pending Support _____

m. Cost Proposal _____

n. Company Commercialization _____

o. Agreement between the Small Business and Research Institution _____

SUBJECT/WORD INDEX TO THE DARPA FY2004 STTR TOPICS

Subject/Keyword	Topic Number
Analog Photonics.....	.003
Coated Conductor.....	.002
Cooling.....	.001
Cryogenics.....	.002
Design for Fabrication.....	.004
Electrocaloric.....	.001
Electro-optic Modulator.....	.003
Ferroelectric.....	.001
Flexible Processing.....	.004
Flexible Substrate.....	.005
HTS Wire.....	.002
Linearization Compensation.....	.003
Magnetocaloric.....	.001
Manufacturing Optimization.....	.004
Microelectronics Fabrication.....	.004
Power Circuits.....	.002
Power Density.....	.002
Power Devices.....	.002
Power Electronics.....	.002
Predistortion Linearizer.....	.003
Process Optimization.....	.004
Refrigeration.....	.001
RF Photonics.....	.003
Sensor Array.....	.005
Superconducting Motors and Generators.....	.002
Thermoacoustic.....	.001
YBCO.....	.002

DARPA 04 STTR Topic List

ST041-001	Solid State Heat Pumps
ST041-002	Cryogenic Power Electronics
ST041-003	Adaptive Broadband Linearization for Analog Photonic Links
ST041-004	Software Tools for Agile Microelectronics Manufacturing
ST041-005	High Performance Transistors on Flexible Substrates

DARPA 04 STTR Topic Descriptions

ST041-001

TITLE: Solid State Heat Pumps

TECHNOLOGY AREAS: Materials/Processes

OBJECTIVE: Design a prototype for a novel light weight solid state cooling system with high reliability.

DESCRIPTION: Thermoacoustic Stirling cycle coolers (1, 2) use acoustics power to pump heat from low temperature to higher temperature sinks. They typically operate by transferring the adiabatic heat of compression of an acoustic wave in a high pressure helium chamber with a heat-transfer stack. The objective of this topic is to design a prototype for an all solid state heat pump which combines the functions provided by the high pressure gas chamber and the heat transfer stack. Thermoelectric cooling devices are not of interest for this topic since significant work has already been funded for this technical approach. The thermoacoustic refrigeration systems move thermal energy like a bucket brigade along the heat transfer stack. Materials developed for magnetic refrigeration (3-6) might be useful in designing solid state heat pumps. Electrocaloric materials (materials which change temperature on application of an electric field or on depolarization) are also of potential use although much less work has gone on in their development. Ferroelectric materials with field induced first order phase transformations may be designed to have a high electrocaloric figure of merit. It may also be possible to design devices which transfer heat via acoustic waves through the electro-mechanical transduction. For the purposes of this topic, the design parameters (temperatures of source and sink, and cooling capacity) will be identified in the proposal based on anticipated applications. For example, 300 watts pumped between 50 degrees centigrade and 21degrees centigrade will be needed for cooling an individual soldier wearing chemical-biological protective gear. Quantitative performance goals for the proposed application must be stated in the proposal along with competitive benchmarks for conventional cooling approaches.

PHASE I: Complete the preliminary design for a solid state heat pump with no moving parts. The design should include a thermodynamic model, identification of the materials of construction along with their figures-of-merit for the system level performance, and the control circuit for operation of the device as appropriate. The preliminary design should also include a detailed physics based computer-aided design model to predict the performance of the heat pump and benchmark against alternative heat pump systems.

PHASE II: Build a testable prototype as designed in Phase I and measure its performance. The prototype should be fully instrumented and flexible enough to explore the control parameters (Voltage, frequency, magnetic field, temperature, etc.) on performance metrics (efficiency, weight specific cooling capacity, etc.).

PHASE III Dual Use Applications: Compact, reliable, environmentally green and efficient cooling devices will have application in automotive and home air conditioning and heating systems. Industrial applications include cooling of semiconductor chips. The potential to replace conventional systems which leak ozone depleting chlorofluorocarbons is significant. Defense applications include thermal management onboard satellites, coolers for IR focal plane arrays, and cooling for personnel in chemical-biological protective suits.

REFERENCES:

1. Steven L. Garrett and Scott Backhaus, "The Power of Sound", American Scientist, November-December 2000, Volume 88, No. 6 <http://www.americanscientist.org/template/AssetDetail/assetid/21006>.
2. R.S. Reid, G.W. Swift, Experiments with a flow-through thermoacoustic refrigerator, J. Acoustic Soc. Am., Volume 108 (6) December 2000, pp. 2835-2842.
3. K. A. Gschneider Jr., V.K. Pecharsky. A.O. Pecharsky, and C.B. Zimm, Recent Developments in Magnetic Refrigeration, Materials Science Forume, Vols. 315-317 (1999), 'Rare Earths '98', pp. 69-76.
4. O. Tegus, E. Brück, K.H.J. Buschow and F. R. de Boer, Transition-metal-based magnetic refrigerants for room-temperature applications, Nature, Vol. 415, January 2002, pp. 150-152.
5. P. Sande, L.E. Hueso, D.R. Miguéns, and J. Rivas, Large magnetocaloric effect in manganites with charge order, App. Phys. Letters, Vol. 79, Number 13, Sept. 24, 2001, pp. 2040-2042.
6. C. Hincinschi, E. Burzo, and J.P. Deville, Magnetic and Magnetocaloric Properties of La_{1.4}-xY_bCa_{1.6}Mn₂O₇, Materials Science Forum, Volume 373-376, 'EMMA-2000', 2001, pp. 521-524.

KEYWORDS: Cooling, Ferroelectric, Electrocaloric, Magnetocaloric, Refrigeration, and Thermoacoustic.

ST041-002

TITLE: Cryogenic Power Electronics

TECHNOLOGY AREAS: Air Platform, Ground/Sea Vehicles, Materials/Processes, Electronics, Weapons

OBJECTIVE: Develop novel cryogenic power electronic materials and devices, develop AC-compatible second generation (2G) high-temperature superconducting (HTS) wire, and optimize existing high-power electronic devices and circuits for cryogenic operation above 60 K. This technology development will enable an order of magnitude decrease in losses for some large DoD power conversion systems, significant improvement in power density, and signature reduction.

DESCRIPTION: Electric power has become increasingly critical for our military preparedness. There has been a tremendous push within the Navy and the Air Force toward significantly more electric power on-board ships, aircrafts, and eventually satellites for propulsion, weapons systems, and sensors. As a result, there is a trend toward utilizing cryogenic technologies in applications where size, weight, and performance are the key drivers, such as propulsion motors and power generators. The goal of this effort is to develop novel cryogenic power technologies that will enable an order of magnitude decrease in losses for large power conversion systems, and significant improvement in power density. This STTR will focus on three technologies: (1) new materials for cryogenic power electronics, such as Silicon Germanium (SiGe) heterostructures; (2) low AC-loss coated conductor for operation above 60K; and (3) high-power electronic devices and circuits optimized for cryogenic operation. This project will address the materials science and device technology challenges critical to the development of significantly smaller, more efficient, lower noise, and more reliable power systems. In particular, SiGe high power switches will be optimized for operation at cryogenic temperatures and will be demonstrated in small power modules.

PHASE I: (1) Perform a feasibility study to examine the potential of novel power electronic materials, such as SiGe heterostructures, for power applications at cryogenic temperatures. Show the feasibility of developing a cryogenic power diode. (2) Design a Yttrium Barium Copper Oxide (YBCO) conductor with low AC losses at 60 Hz and 500 Hz. (3) Study and quantify the advantage of a select silicon power circuit optimized for cryogenic operation.

PHASE II: (1) Design, fabricate, and demonstrate a cryogenic high-power switch (e.g., Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET), or Insulated Gate Bipolar Transistor (IGBT) in a novel power electronic material, such as SiGe heterostructures. The goal is to achieve an order of magnitude improvement in the speed and an order of magnitude reduction in losses relative to corresponding room temperature silicon power devices. (2) Demonstrate 2G YBCO wire with AC losses better than half the losses of the equivalent Bismuth Strontium Calcium Copper Oxide (BSCCO) wire. (3) Design and demonstrate a cryogenic power circuit for a specific DoD application, such as a propulsion motor controller.

PHASE III Dual Use Applications: The technology development under this STTR can be used to provide very compact power control and distribution systems for the next generation of Naval vessels equipped with electric weapons and electric drive as well as for proposed electrically powered airborne weapons systems. In the civilian sector this technology will be important for power conversion equipment in power utilities as well as for cryogenic medical instrumentation, such as Magnetic Resonance Imaging (MRI).

REFERENCES:

1. R. Singh and B. J. Baliga, *Cryogenic Operation of Silicon Power Devices*, Boston: Kluwer Academic (1998).
2. F. Hirose, Y. Souda, K. Nakano, S. Goya, T. Nishimori and S. Okumura, "New SiGe bipolar transistors and p-i-n diodes for power switching," *IEEE Tr. Electron Devices*, 48, p. 2417-2420, Oct. 2001.
3. D. Larbalestier, A. Gurevich, D. M. Feldmann, and A. Polyanskii, "High-Tc superconducting materials for electric power applications", *Nature*, vol. 414, p. 368 (2001).

KEYWORDS: Power Electronics; Cryogenics; Superconducting Motors and Generators; Power Density; Power Devices; Power Circuits; Coated Conductor; HTS Wire; YBCO.

TECHNOLOGY AREAS: Sensors, Electronics

OBJECTIVE: Develop broadband photonic link linearization techniques/circuits for wideband analog electro-optic transmission applications.

DESCRIPTION: Adaptive wide-bandwidth linearization compensation is needed for low-cost analog photonic links in many DoD communications, radar, munitions, and weapon platform applications. The compensation needs to be real-time adaptive in order to maintain linearity over varying input signal bandwidth, power levels and temperature variations.

The linearity requirements of high-speed analog photonic modulation schemes vary widely for commercial (cable TV (CATV), wireless cellular antenna remoting) and DoD (radio frequency (RF) photonic links) applications. Demanding analog applications, including both CATV and DoD systems, require moderate to high linearity (100 to 130 dB per unit Hz in spurious-free dynamic range, or SFDR). On the commercial CATV side, the linearization problem is made easier by the fact that lower operating frequencies (<1 GHz) and fixed signal input levels are utilized. Linearized photonic links for CATV signal distribution have been in the field (both direct modulation and external modulation) for over 10 years. Military deployment of linearized analog photonic links is far less developed. Reasons for this include the fact that many military applications require frequency coverage well beyond 1 GHz (>20 GHz in many cases) and require uncompromised RF performance in a dynamically changing signal environment. The combination of wide, multi-octave frequency ranges and varying input signal conditions poses a significant RF challenge to the military system and component designers/developers, especially in terms of maintaining high linearity.

Direct laser diode modulation is attractive because it is the most compact, and usually the lowest-cost, solution. High linearity has been achieved in static direct modulation CATV links (<1 GHz) using electronic predistortion linearization. From a military application perspective, drawbacks to this commercially deployed technology include the limited frequency range and minimal adaptivity (only temperature compensation). This is especially limiting for antenna receiver applications where changing signal environments and large signal strength variations are routinely encountered. Laser diode linearization can be useful for military applications at higher frequencies provided high-speed lasers are available and a broadband adaptive linearizer can be achieved. Extending the frequency range of linearized laser diode links well beyond 10 GHz becomes challenging due to fundamental laser relaxation frequency considerations. As techniques to extend the laser modulation bandwidths become available, linearized laser diode links using optical or electrical domain linearization approaches become viable.

For even larger bandwidths extending out beyond 40 GHz, integrated optical modulators, either lithium niobate or semiconductor based are attractive candidates. Lithium niobate Mach-Zehnder Modulators (MZMs) are the most mature broadband modulator technology. Semiconductor electro-absorption modulators (EAMs) and MZMs, which can be directly integrated with a semiconductor laser source, represent another class of broadband optical modulators currently being developed. Modulation bandwidths exceeding 40 GHz have been demonstrated with both lithium niobate and III-V semiconductor optical modulators. Due to their inherent nonlinear transfer functions, linearity is an issue with both these broadband modulator candidates that must be addressed. As with laser diode modulation, either optical domain or electrical domain linearization techniques can be employed to improve the broadband SFDR (both 2nd and 3rd order distortion compensation). Adding momentum to the case for external modulation is the fact that high sensitivity links have already been demonstrated using lithium niobate and semiconductor optical modulators. If these high frequency, low noise figure links can be robustly coupled with high linearity, many military transmission and signal processing applications are enabled.

Developing a robust broadband modulator (or laser diode) linearization approach that is adaptive in real-time and can operate to bandwidths well beyond 1 GHz is the thrust of this research and development topic. Either optical or electrical domain link linearizers, or a combination of the two is acceptable provided a development path to low-cost manufacturing can be demonstrated. Recent work has shown the promise of achieving adaptive linearization compensation for analog photonic links at lower frequencies (<1 GHz) using both electrical domain and optical domain techniques. Based on these developments, new broadband linearization approaches and optoelectronic integrated circuits (OEICs) are solicited to tackle the challenge of multi-GHz bandwidths and instantaneous adaptive

feedback (through optical and/or electrical compensation). Novel broadband linearization techniques for both laser diode and integrated optic modulator based photonic links will be considered, provided that wide bandwidth operation is achievable (18 GHz Phase II demonstration target). Emphasis will be placed on wideband linearization techniques that show the most potential for operating in a dynamic signal/temperature environment with uncompromised RF link performance.

PHASE I: Propose a feasibility study to investigate, model, and perform critical experiments to identify possible low-cost adaptive compensation approaches with real time feedback to achieve wideband linear operation of analog photonic links. An operating bandwidth of 18 GHz should be targeted.

PHASE II: Develop low-cost adaptive linearization compensation OEIC. Demonstrate performance with optical modulators (or laser diode) with DC to 18 GHz input signals for multi-tone RF signal remoting applications. Design a unit for an OEIC link linearizer which can be manufactured and qualification tests be performed to validate the design and its performance.

PHASE III Dual Use Applications: Some specific military uses include high bandwidth, multi-wavelength, fiber-optic signal transmission systems as well as optical time delay modules for broadband signal processing and phased-array beam steering applications. Fiber radio for cellular access has become a significant commercial market. With the drive to offer broad-band wireless access, it is very likely that the market share of fiber-radio access systems will grow further. Now that the majority of fixed communication is by optical fiber, and per-channel data rates are rising through 40 Gb/s, the need for analog microwave photonic technology in this large market is assured.

REFERENCES:

1. "Use of RF Photonics in Next Generation Military Antenna Systems", S. Pappert, Department of the Navy, SPAWAR Systems Center, San Diego (SSC-SD), DARPA AOSP Study Group, December 6, 2000. <http://www.darpa.mil/mto/aosp/workshop/pappert.pdf>.
2. "Advances in Traveling-Wave Electro-absorption Modulators for Analog Applications", P. K. L. Yu, W. S. S. C. Chang, Y. Zhuang, University of California, San Diego, CA, USA and G. Li, Agere Systems, Breinigsville, PA, USA, The 15th Annual Meeting of the IEEE Lasers and Electro-Optics Society, 10 - 14 November 2002, Glasgow, Scotland.
3. "Analog Modulation of Semiconductor Lasers," J. Piprek and J. E. Bowers, Chapter 3 in RF Photonic Technology in Optical Fiber Links, ed. W. Chang, Cambridge University Press (2002).
4. "Broad-band electronic linearizer for externally modulated analog fiber-optic links", Chiu, Y.; Jalali, B.; Garner, S.; Steier, W., IEEE Photonics Technology Letters, vol. 11, Jan. 1999, pp. 48-50.
5. "Electronic linearization of fiber optic links (Predistortion Linearizer), R. Sadhwani, J. Basak, and B. Jalali", Proceedings of Optical Fiber Communication Conference (OFC 2003), Atlanta, GA, March 2003, in press.
6. "High Speed Optical Modulators with Predistortion Compensation", T. Chu, E. Yablonovitch, RF Photonics Materials and Devices MURI Review, 1998, http://www.ee.ucla.edu/~laser/MURI/view_graphs/muri98/yablonovitch98/sld001.htm.

KEYWORDS: Linearization Compensation, Predistortion Linearizer, Analog Photonics, Electro-optic Modulator, RF Photonics.

ST041-004

TITLE: Software Tools for Agile Microelectronics Manufacturing

TECHNOLOGY AREAS: Information Systems, Materials/Processes, Sensors, Electronics

OBJECTIVE: Develop software tools for flexible processing that enable cost-effective production scalability and also improves the capabilities of tools and processes to yield high performance but low volume semiconductor components.

DESCRIPTION: This topic seeks to develop software tools for modeling and solving the challenges of obtaining high performance, leading-edge microelectronics cost-effectively at low volume. A number of integrated circuits that are of potential interest to the military or are needed in defense systems are implementations of sophisticated designs, high in performance but low in product volumes. Merchant semiconductor fabrication has evolved toward

large processing facilities that are optimized for high volume production. The high costs and risks associated with constructing and operating these factories has led to fabrication processes that are somewhat limited in flexibility. In addition, the design process for accessing these high volume factories has conservative limitations to preserve process margins. Semiconductor fabrication at the leading-edge tends to be the most cost-effective for high volume products where non-recurring costs such as masks are amortized over large product volumes. The high volume factories typically have high volume tools and sophisticated computer-integrated manufacturing to balance wafer flows and work in progress. To improve the production of small volume chips, new software tools need development that can identify new tool throughput[1] or process capabilities[2], balance less than full capacity in high volume tools, more closely couple design and processing, and generally reduce the cost of low volume high performance components. This topic will develop the tools necessary to understand how to obtain high performance, leading-edge integrated circuits from flexible factories. Other benefits could accrue due to the use of smaller, more efficient and flexible factories with smaller capital costs, yet still capable of leading-edge production in scaleable volumes.

PHASE I: Determine feasibility of the overall software-based approach for enabling flexible manufacturing at the state-of-the-art. As appropriate, obtain requirements to determine the ability to use software tools to solve small volume semiconductor manufacturing problems, including optimization of process and degrees of flexibility. Determine critical barriers for acceptance and design experiments to overcome those barriers.

PHASE II: Develop the novel software tools for agile microelectronics manufacturing. Initial software tool development will be followed by simulation of the process to validate the approach and to assess potential impact on component performance and cost. The experiments designed under Phase I should be implemented as appropriate and are necessary to validate the approach. The benefits of incorporation of these tools for small volume fabrication should be quantified.

PHASE III Dual Use Applications: The development of viable sources of small volume custom chips will have an enormous impact both in the military and civilian markets for providing leading-edge technology capabilities for small volume markets. Many embedded industrial electronic applications use specialty chips and sensors. The software tool developed under this topic would enable cost-effective manufacture of small volume parts in high volume or flexible microelectronics foundries, potentially enabling huge markets for small orders of advanced microelectronics for industrial, commercial, and military systems.

REFERENCES:

1. Jacobs, J.H., Etman, L.F.P., Rooda, J.E., Van Campen, E.J.J., Quantifying operational time variability: the missing parameter for cycle time reduction, Advanced Semiconductor Manufacturing Conference, 2001, 1-10.
2. Schneider, C., Smyth, J., Watts, A., Automated photolithography critical dimension controls in a complex, mixed technology, manufacturing fab, Advanced Semiconductor Manufacturing Conference, 2001, 33-40.

KEYWORDS: Microelectronics Fabrication, Manufacturing Optimization, Flexible Processing, Design for Fabrication, Process Optimization

ST041-005

TITLE: High Performance Transistors on Flexible Substrates

TECHNOLOGY AREAS: Materials/Processes, Electronics, Battlespace

OBJECTIVE: Identify and develop innovative technology to enable high performance (>10 GHz) transistor based devices on flexible substrates.

DESCRIPTION: Phased array radar and terahertz antennas provide beamforming capabilities and directional signal origin capabilities that convey a great benefit on the battlefield. The tightness of the beam and the angular resolution of the signal location depend on the physical size of the array with meter sizes needed for many applications. For these frequencies, fast switching is necessary and at present this is the only possible used compound semiconductor based devices. In order to produce a long baseline antenna array, the devices, formed by lithography on single crystal substrates, are placed at their desired position and interconnected. This technique is inherently costly and has been limited to portable systems which are relatively small. A more scalable method

would be to print the devices and interconnects directly on the flexible substrate of the desired size¹. Printing techniques have been demonstrated on large flexible substrates but the best performing devices, based on polysilicon, are still orders of magnitude too slow for radar uses (>10 GHz). Innovative new materials or processes will be needed in order to enable devices which can handle the GHz frequencies of radar systems. In addition, methods must be developed to manufacture devices of the required complexity².

PHASE I: Conduct a feasibility study on high performance transistor fabrication on flexible substrates. Identify materials and techniques that have the potential to produce large area antenna arrays.

PHASE II: Develop the materials and methods identified in Phase I and demonstrate a proof-of-concept array element.

PHASE III Dual Use Applications: The technology developed under this STTR can be used in commercial and military low cost communication devices.

REFERENCES:

1. Wu, M., Chen, Y., Pangal, K., Sturm, J.C., Wagner, S., High-performance polysilicon thin film transistors on steel substrates, *J. Non-Cryst. Solids* 266-269, 2000, 1284-1288.
2. Fulks, R.T., Ho, J., Boyce, J.B., A New Laser-Processed Polysilicon TFT Architecture, *IEEE Elec. Dev. Lett.*, 22, 2001, 86-88.

KEYWORDS: Sensor Array, Flexible Substrate.