Executive Summary

Unified Avionics Interconnect Standard

Using Byte Addressable Scaleable Coherent Interface/ Real Time (SCI/RT)

PNUM 24A and 24B

Background: SCI is one of the candidates for the Joint Strike Fighter (JSF) interconnect network with a goal to implement a Unified Avionics Interconnect. SCI is one of the standard interconnects potentially meeting JSF requirements, and hence capable of replacing five separate interconnects currently used in the F-22. It was selected by the Society of Automotive Engineers (SAE) Avionics Division, Unified Network Interconnect Task Group (UNIT) as the basis for their unified interconnect standard.

The low latency of SCI is due to its byte addressability feature allowing SCI to transfer data over a network without invoking software, in a manner analogous to that of backplane buses such as PCI. Node addressable networks (Ethernet, Fibre Channel, etc.) require that software be invoked in every transfer greatly increasing total latency. Lockheed is continuing their SCI interconnect development with a low power, all CMOS, system.

Other potential users include the Integrated Sensor Subsystem Program, currently using SCI to interconnect digital components; the Canadian Navy, which has developed a prototype signal processor using SCI, and the Norwegian Defense Research Establishment, which has done several SCI projects including radar signal processing. Commercial real time system developers such as the telecommunications industry are also potential SCI users.

A related effort is that of the 1394 Trade Association (Firewire) to extend SCI to become their next generation interconnect as IEEE 1394.2 (Serial Express). The most active participants of this group are from Sun and Apple. It is their intent to develop a byte addressable network to connect workstations together and also to connect peripherals to workstations. A potential advantage of this approach is sharing memory between peripherals and the PC/workstation so that peripherals become cheaper because they can use the PC/workstation memory rather than requiring their own. In addition, the 1394 group wants to add an isochronous capability to SCI to better support voice and video multi-media. The results of this effort could feed into SCI/RT.

Objectives: The overall objective of this effort is to establish a modular open system architecture (OSA) for military systems based on a byte addressable unified avionics interconnect standard. The interconnect requirements are high throughput (to support future digital receiver, and other, technology), very low latency (to support emerging Ghz processors), distance insensitivity (to allow both backplane and LAN usage), and support for both message passing and shared memory computing paradigms (for universal applicability). The baseline for the interconnect is the Institute of Electrical and Electronic Engineers (IEEE) 1596 Scaleable Coherent Interface (SCI). The SCI standard is complete and being applied to high performance commercial "server computers" (Sequent, Hewlett Packard (HP), and Data General) and workstation interconnects (Sun and Dolphin). This effort seeks to extend the base SCI standard for real time and military usage.

It seeks to add, and standardize, enhancements for real time and military usage to the base SCI (or 1394.2) protocol in the areas of determinism, fault tolerance, and security. Current military systems have worked around these difficulties by limiting the system configuration, lightly loading the interconnect, and adding their own special features. A better approach is to add standardized features to support these needs. The IEEE P1596.6 SCI/RT Working Group and the SAE Unified Network Interconnect Task Group are working toward this standardization. Several protocol enhancements have been proposed for SCI/RT which are being simulated and evaluated.. The University of Florida High Performance Computer Laboratory is currently performing most of these simulations. Edgewater Computer, the original developer of the SCI/RT concept, is doing analysis and some limited additional simulations.

Related Activities: Three Small Business Innovative Research (SBIR) projects related to SCI. The first SBIR seeks to develop a low cost, 4 to 8 Gbits/sec, serial fiber network interconnect. This interconnect would work with SCI. The second SBIR is to prototype the SCI/RT interface chip. The third SBIR seeks to develop a low latency, low cost, processor direct network interface and a very low latency CORBA standard interface. This SBIR would also be directly compatible with SCI.