DEFENSE THREAT REDUCTION AGENCY
12.1 Small Business Innovation Research (SBIR)
Proposal Submission Instructions

The mission of the Defense Threat Reduction Agency (DTRA) is to safeguard the United States and its allies from weapons of mass destruction (WMD) – chemical, biological, radiological, nuclear and high-yield explosives – by providing capabilities to reduce, eliminate and counter the threat and mitigate its effects. This mission includes research and development activities organized into chemical/biological, nuclear, counter WMD, and innovation/systems engineering technology portfolios. The activities described herein are drawn from DTRA's nuclear, counter WMD, and innovation/systems engineering portfolios. Communications for this program should be directed to:

Defense Threat Reduction Agency
ATTN: Mr. Robert Swahn, SBIR Program Manager
8725 John J. Kingman Drive, MSC 6201
Fort Belvoir, VA 22060-6201
E-mail: dtrasbir@dtra.mil (use of e-mail is encouraged)

The DTRA SBIR program complements the agency's principal technology programs to detect/locate/track WMD; interdict or neutralize adversary WMD capabilities; protect against and restore following WMD use; attribute parties responsible for WMD attacks; and provide situational awareness and decision support to key leaders. SBIR topics reflect the current strategic priorities where small businesses are believed to have capabilities to address challenging technical issues. DTRA supports efforts to advance manufacturing technology through SBIR, where the challenges of such technology are inherent to technical issues of interest to the agency.

PROPOSAL PREPARATION AND SUBMISSION

Paragraph 3.0 of the SBIR Program Solicitation (found at http://www.dodsbir.net/solicitation/) provides the proposal preparation instructions. Consideration is limited to those proposals which do not exceed $150,000 and seven months of performance. Proposals may define and address a subset of the overall topic scope. Proposals applicable to more than one DTRA topic must be submitted under each topic.

PROPOSAL REVIEW AND EVALUATION

During the proposal review process, employees from BRTRC, Inc., and TASC, Inc., will provide administrative support for proposal handling and will have access to proposal information on an administrative basis only. Organizational conflict of interest provisions apply to these entities and their contracts include specifications for non-disclosure of proprietary information. All proposers to DTRA topics consent to the disclosure of their information to BRTRC and TASC employees under these conditions.

BRTRC, Inc.
8260 Willow Oaks Corporate Drive, Suite 800
Fairfax, VA 22031-4506

TASC, Inc.
8211 Terminal Road, Suite 1000
Lorton, VA 22079-1421

DTRA will evaluate Phase I proposals using the criteria specified in paragraph 4.2 of the Program Solicitation. Topic Points of Contact (TPOC) lead the evaluation of all proposals submitted in their topics.

SELECTION DECISION AND NOTIFICATION

DTRA has a single Source Selection Authority (SSA) for all proposals received under this solicitation. The SSA either selects or rejects Phase I proposals based upon the strengths and weaknesses identified in proposal review plus other considerations including limitation of funds and balanced investment across all the DTRA topics in the solicitation. Balanced investment includes the degree to which offers support a manufacturing technology challenge. To balance investment across topics, a lower rated proposal in one topic could be selected over a higher rated proposal in a different topic. DTRA reserves the right to select all, some, or none of the proposals in a particular topic.

Following the SSA decision, the contracting officer will release notification e-mails through DTRA's SBIR evaluation system for each accepted or rejected offer. E-mails will be sent to the addresses provided for the Principal Investigator and Corporate Official. Offerors may request a debriefing of the evaluation of their proposal. Once released, debriefings are viewable at https://www.dtrasbir.net/debriefing/ and require password access. Debriefings are provided to help improve the offeror's potential response to future solicitations. Debriefings do not represent an opportunity to revise or rebut the SSA decision.

For selected offers, DTRA will initiate contracting actions which, if successfully completed, will result in contract award. DTRA Phase I awards are issued as fixed-price purchase orders with a seven-month period of performance. DTRA may complete Phase I awards without additional negotiations by the contracting officer or opportunity for revision for proposals that are reasonable and complete.

DTRA's projected funding levels support a steady state of eighteen Phase I awards annually over multiple solicitations. Actual number of awards may vary.

DTRA Phase I awards for this solicitation will be fully funded with FY12 appropriations available on or after December 1, 2011. Awards will be subject to availability of those funds and are expected to occur during the second and/or third quarter of FY12. DTRA manages SBIR as an ongoing program and does not classify individual Phase I awards as new program starts for the purpose of Continuing Resolution Authority.

CONTINUATION TO PHASE II

Only Phase II proposals provided in response to a written invitation from a DTRA contracting officer will be evaluated. DTRA invitations are issued based on the degree to which the offeror successfully proved feasibility of the concept in Phase I, program balance, and possible duplication of other research. Phase II invitations are issued when the majority of Phase I contracts from the preceding solicitation are complete. Phase I efforts which were delayed in award or extended after award will be considered for invitation the following year. DTRA is not responsible for any money expended by the proposer prior to contract award.

DTRA's projected funding levels support a steady state of six to eight new Phase II awards annually to meet an objective of continuing approximately fifty percent of Phase I efforts to Phase II. Actual number of awards may vary.

OTHER CONSIDERATIONS

DTRA does not utilize a Phase II Enhancement process. While funds have not specifically been set aside for bridge funding between Phase I and Phase II, DTRA does not preclude FAST TRACK Phase II awards, and the potential offeror is advised to read carefully the conditions set out in this solicitation.

Notice of award will appear first on the Agency Web site at http://www.dtra.mil. Unsuccessful offerors may receive debriefing upon written request only. E-mail correspondence is considered to be written correspondence for this purpose and is encouraged.

DTRA SBIR 12.1 Topic Index

DTRA SBIR 12.1 Topic Descriptions

DTRA121-01 TITLE: Develop a Cost Efficient and Effective Method for Cast-In-Place Ultra High Performance Concrete (UHPC)

TECHNOLOGY AREAS: Materials/Processes

OBJECTIVE: Develop a cost effective and efficient method to mix, cure, place, and transport large scale, cast-in-place fiber reinforced (FR) UHPC structures having a minimum compressive strength of 25 kilo pounds/in 2 (ksi) and sustained postcracking tensile strength of 0.72 ksi.

DESCRIPTION: The Defense Threat Reduction Agency (DTRA) seeks development of materials and methods for mixing, placing and curing large cast-in-place FR UHPC structures outside of a laboratory environment. With the lack of large aggregate in current formulations of UHPC, achieving sufficient shear in mixing is a challenge. Likewise, transportation and placement of UHPC has challenges unique to this material. Finally, the curing treatment applied to concrete—which is always important—is even more important in the case of FR UHPC. However, steam treatment of FR UHPC in a controlled environment may not always be feasible or even desirable. DoD could benefit from a low cost method for emplacing FR UHPC in field environments, both for force protection applications, and for creation of targets for munitions testing programs. Process should define materials (e.g., concrete constituents, form and cover materials, heaters, steamers, shear mixers, etc.) needed and process steps taken (e.g., steaming begins when and for how long and at what conditions) to achieve desired material characteristics with a field placement.

PHASE I: Development of proof of concept for a cast-in-place method that may be feasible and cost effective for placement of large FR UHPC pours resulting in high compressive strength similar to laboratory cured FR UHPC samples.

PHASE II: Develop materials and process methods necessary to achieve high compressive strength FR UHPC structural components. Demonstrate field placement for a large FR UHPC pour to show feasibility of meeting minimum compressive strength requirement with cast-in-place UHPC.

PHASE III DUAL USE APPLICATIONS: Developed/advanced products and methodologies to help place FR UHPC in the field for target testing or force protection purposes.

REFERENCES:
1. US Department of Transportation Federal Highway Administration, “Material Property Characterization of Ultra-High Performance Concrete,” Publication No. FHWA-HRT-06-103, 2006 August

2. US Department of Transportation Federal Highway Administration, “Material Property Characterization of Ultra-High Performance Concrete,” 2008 December 4, http://www.tfhrc.gov/structur/pubs/06103/ref.htm

3. US Department of Transportation Federal Highway Administration, “Ultra-High Performance Concrete,” Publication No. FHWA-HRT-11-038, 2011 March

KEYWORDS: Ultra High Performance Concrete, steel fiber, cast-in-place, concrete curing, reactive powder concrete, fiber reinforced concrete

DTRA121-02 TITLE: The Characterization and Mitigation of Radiation Effects on Nano-technology Microelectronics

TECHNOLOGY AREAS: Materials/Processes, Sensors, Electronics, Nuclear Technology

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), which controls the export and import of defense-related material and services. Offerors must disclose any proposed use of foreign nationals, their country of origin, and what tasks each would accomplish in the statement of work in accordance with section 3.5.b.(7) of the solicitation.

OBJECTIVE: The successful outcome of this effort will support the use of ultra-deep submicron integrated circuits in satellite systems that will result in very significant savings in weight, power and reliability for systems that include Space Radar, Space Tracking and Surveillance Systems and others. In addition, this effort will also support the use of compound semiconductor technologies (e.g. III-V based devices: antimony compound semiconductors, indium phosphate, and others) in these systems and their introduction into advanced spacecraft and missile systems with similar savings in both power and weight, coupled with increased performance.

DESCRIPTION: Current satellite systems are fabricated using a mix of commercial and radiation hardened circuits. However, the use of advanced commercial integrated circuits devices results in added complexity to mitigate radiation effects that can result in the miss-operation and/or destruction of devices. In many cases, the penalties in increased power, area, weight and added circuit complexity out-weigh any potential benefits and preclude the use of the advanced commercial technology. Moreover, these technologies have demonstrated sensitivity to radiation effects.

The current methods to mitigate radiation effects, while proven to be effective at circuit geometries > 150 nm silicon based technology, have been shown to be less effective when applied to integrated circuit feature sizes below 100 nm silicon based and compound semiconductor technologies. In addition, the introduction of new technologies, e.g. quantum function circuits, will require the development of new mitigation approaches. Thus, if minimally invasive methods such as the use of alternative materials, circuit enhancements, and other innovative approaches could be developed to reduce radiation effects sensitivity these devices could be used with little or no penalties.

Therefore, the basic approach to accomplish this task would be to leverage commercial microelectronics at the $\leq$ 32nm nodes and augment these technologies with radiation mitigation techniques that would have minimal impact on the electrical performance and manufacturability. This same approach also applies to the radiation hardening of the compound semiconductor and other technologies.

Additionally, the development of such methods requires the development of cost effective methods and or design techniques to model and simulate the radiation response of these $\leq$ 45nm, compound semiconductor and other technologies. Without a robust modeling and simulation capability it would be both technically and economically unfeasible to develop these mitigation methods.

PHASE I: The offeror will identify innovative, nontraditional, to include material approaches, computational methods, novel algorithms or novel transistor structures (3D Structures, Finfet etc.), to mitigate radiation effects in: $\leq$ 32nm CMOS microelectronics technologies; $\leq$180nm III-V; $\leq$ 130nm SiGe; $\leq$ 180nm SiC; graphene; CNT and other exotic material solutions. Develop computational methods and/or novel algorithms to convert 2D designs to 1D designs methodologies. Development of cost effective radiation effects modeling and simulation methods for $\leq$ 32nm microelectronics, compound semiconductor and other technologies for digital and analog/mixed-signal microelectronics applications will be conducted. Proof-of-concept design approaches to mitigate radiation effects will be identified. Development of faster, cost effective algorithms to model and simulate $\leq$ 32nm microelectronics, compound (III-V, SiGe, SiC, graphene, CNT) semiconductor and other technologies for digital and analog/mixed-signal microelectronics applications will be conducted. Proof-of-concept design approaches to mitigate radiation effects will be identified. Identification of design science approaches to mitigate radiation effects and testing and evaluation methodology to mitigate radiation effects will be identified.

PHASE II: The offeror will develop the identified innovative, nontraditional, to include material approaches, computational methods, novel algorithms or novel transistor structures, to mitigate radiation effects (3D Structures, Finfet etc.), to mitigate radiation effects in: ≤ 32nm CMOS microelectronics technologies; ≤ 180nm III-V; ≤ 130nm SiGe; ≤ 180nm SiC; graphene; CNT and other exotic material solutions. Development of faster cost effective radiation effects modeling and simulation methods for the identified technologies for digital and analog/mixed-signal microelectronics applications will be conducted. Improve existing or develop Electronic Design Automation (EDA) tools (programs) that can: Identify and mitigate design sensitivities in complex integrated circuits for innovative nontraditional solutions. Perform trade studies to provide optimized integrated circuits with respect to radiation and electrical performance for innovative nontraditional solutions. Perform trade studies to model reliability of system architectures using unreliable components. Perform virtual Monte Carlo radiation test benching/simulation of complex integrated circuits. The incorporation of predictive radiation response models into high-level abstractions. Perform radiation-hardened-by-designs (RHBD) trade studies from one feature size to another, (e.g. 90nm to 45nm etc.). Perform failure mode reconstruction in complex circuits from test data for innovative nontraditional solutions. Develop novel algorithms for design space exploration for innovative nontraditional solutions.

The offeror will develop or improve the existing Technology Computer Aided Design (TCAD) tools that can: Provide cost effective 3-D models to support the simulation of the radiation response of nanotechnology microelectronics. Identify radiation sensitivities at the transistor level. Develop or improve the existing Mixed-Mode and Level Simulation systems that can effectively couple the radiation response at the transistor level to higher levels of circuit and subsystem integration to support the accurate radiation response simulation up to and including the sub-system level.

The offeror will develop and demonstrate design science approaches for mitigation of radiation effects for ≤ 45nm radiation effects modeling and simulation methods for these technologies.

PHASE III DUAL USE APPLICATIONS: Use of the mitigation, modeling and simulation methods developed through this effort will support the use of advanced microelectronics for terrestrial applications such as very high performance microprocessor, advanced servers, and very large cache memories.

REFERENCES:

1. IEEE Transactions on Nuclear Science; December 2007, Volume 54, Number 6, Session H: Single Event Effects Mechanisms and Modeling, pages 2297 - 2425

2. IEEE Transactions on Nuclear Science; December 2005, Volume 52, Number 6, Session A Single Even Effects: Mechanisms and Modeling, pages 2104-2231

3. IEEE Transactions on Nuclear Science; December 2005, Volume 52, Number 6, Session F Single Even Effects: Devices and Integrated Circuits, pages 2421-2495

4. JEDEC 57, SEE Test and Characterization Guidelines and Test Method

5. Military Test Method 1019, Steady State Total Ionizing Dose

6. ASTM 1892 ¨C Steady State Total Ionizing Effects Guideline

KEYWORDS: Single-Event Effects, Single-Event Upset, Single-Event Transients, Total Ionizing Dose, Displacement Damage, nano-technology